REMARKS

Claims 1 - 18 remain active in this application. Claims 14 - 18 have been withdrawn from consideration as being non-elected, with traverse, in response to a requirement for restriction. The specification has been reviewed and editorial revisions made where seen to be appropriate. New claims 19 and 20 have been added to more fully claim the subject matter of the invention. Support for new claims 19 and 20 is found in [Para 28] and [Para 46]. No new matter has been introduced into the application. The indication of allowability of the subject matter of claim 9 is noted with appreciation.

Restriction has previously been required in this application and the requirement was traversed with substantial arguments establishing the impropriety of the requirement in the response filed July 7, 2006. The present action is entirely silent in regard to the requirement or the traverse presented other than the indication on the form PTO-326 that claims 14 - 18 are withdrawn from consideration. It is respectfully submitted that in view of the failure of the Examiner to respond to the previously presented substantial traverse that the requirement has been effectively admitted to be improper for the reasons of record and an action given on all claims in the application. It is also respectfully submitted in this regard that the present office action is also incomplete for that reason and that the next office action cannot properly be made final.

Claims 1 - 2 have been rejected under 35 U.S.C. §103 as being unpatentable over Yamada et al. ('981) in view of Furukawa et al. Claims 3 - 8 and 10 - 13 have been rejected under 35 U.S.C. §103 as being unpatentable over Yamada et al. ('981) in view of Furukawa et al. and

Yamada et al. ('384). Both of these grounds of rejection are respectfully traversed.

The Examiner correctly asserts that Yamada et al. ('981) teaches an integrated circuit including SOI and bulk semiconductor regions with a trench therebetween but admits that Yamada et al. does not teach or suggest providing epitaxial silicon in the trench and relies on Furukawa et al. for teaching epitaxial growth of silicon in a trench. In fact, Yamada et al. appears to teach only polysilicon (column 2, line 20), amorphous silicon (column 2, line 50), SiGe (column 2, line 51) or a dielectric film (column 2, lines 54 - 55) as a boundary layer 47. It is respectfully submitted that this admitted deficiency of Yamada et al. ('981) is not mitigated by Furukawa et al. While Furukawa et al. teaches formation of "single crystalline silicon layer 24 *without grain boundaries*" (column 4, lines 38 - 39 - emphasis added) which is formed as an epitaxial layer (column 4, line 36), it does not teach use of epitaxially deposited material in a trench at a boundary between a SOI region and a bulk semiconductor region but, rather, teaches such a structure wholly within the SOI region and separated therefrom by insulating spacers 22 (which also promote the epitaxial single crystalline layer formation). Moreover, the purpose of this structure in Furukawa et al. is for formation of bulk semiconductor devices (Abstract, penultimate sentence) and thus the structure essentially provides bulk semiconductor regions within the SOI structure which are separated by insulating spacers 22. Thus, correctly viewed, Furukawa et al. does not disclose of teach anything relevant to the claimed invention beyond what is taught in Yamada et al ('981) *which the Examiner has admitted to be insufficient to answer the claim recitations.*

This clear deficiency of the combination of Yamada et al. ('981) and Furukawa et al. is not mitigated by Yamada et al. ('384) and the Examiner has not asserted that it is. Therefore, it is respectfully submitted that the Examiner has clearly failed to make a *prima facie* demonstration of obviousness of any claim in the application. Moreover, while Yamada et al. ('384) is cited to teach formation of claimed junctions, no junctions shown in Figures 2A, 3A or 4C, relied upon by the Examiner, are "butted junctions" or in the recited locations. Additionally in this regard, it is respectfully submitted that the Examiner may not fully understand the invention since the Examiner bases the conclusion of obviousness in regard to the recited junctions on the motivation of improved performance while, in fact, the junctions are provided to engender electrical isolation between the bulk or "handling" substrate without requiring more complex structures and the SOI device layer and is a matter of operability and process simplicity (not provided by the junctions of Yamada et al. ('384)) rather than improved performance of the devices formed (which, in accordance with the invention, largely results from freedom to employ optimal crystal orientations and more reliable connections).

Further, it is respectfully brought to the Examiner's attention that the structure claimed addresses both the problems of different crystal orientations in respective SOI and bulk semiconductor regions and the problems encountered in forming connections between SOI and bulk semiconductor regions with wiring layers; neither of which is contemplated or recognized, much less providing a solution thereto in the prior art relied upon by the Examiner. Both of these problems are addressed by the invention in providing the simple expedient of

providing epitaxial crystalline material in a trench between the respective regions which provides for a transition between crystal orientations if a difference in crystal orientation exists between regions (now explicitly recited in new claims 19 and 20) and supports connections between the respective regions being made using silicide rather than a wiring layer (explicitly recited in original claim 6 which the Examiner does not address). Since neither of these problems are addressed or solutions provided, the prior art relied upon cannot lead to an expectation of success in achieving the unexpected results provided by the invention and thus cannot provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness in regard to the subject matter of any claim in the application.

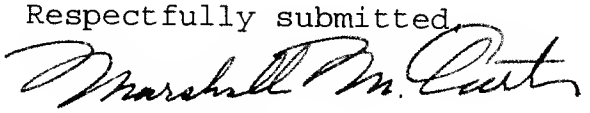
Accordingly, in view of the foregoing, it is clearly seen that the grounds of rejection of record are in error and that no *prima facie* demonstration of obviousness of any claim has been or can be made based on the references relied upon by the Examiner. Therefore, it is respectfully submitted that reconsideration and withdrawal of the currently asserted grounds of rejection is clearly in order and such actions are respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such

action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456 of International Business Machines Corporation (Burlington).

Respectfully submitted,



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